SiC Diode and MOSFET product portfolio
Low stray inductance power module

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Discrete & Integrated Solutions Group

Fortronic, Modena
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# SiC Target Markets and Applications

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<td>• Lighting</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

| **Products** | | | | | |
| • SIC Diodes | • SIC Diodes | • SIC Diodes | • SIC Diodes | • SIC Diodes |
| • SIC MOSFETs | • SIC MOSFETs | • SIC MOSFETs | • SIC MOSFETs | • SIC MOSFETs |
| • Si MOSFETs | • Si MOSFETs | • Si MOSFETs | • Si MOSFETs | • Si MOSFETs |
| • Si IGBT | • Si IGBT | • Si IGBT | • Si IGBT | • Si IGBT |
| • Si Diodes | • Si Diodes | • Si Diodes | • Si Diodes | • Si Diodes |
| • Si/SiC Power Modules | | | • Si/SiC Power Modules | | |

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SiC Discrete MOSFET
Microsemi Next-Generation SiC MOSFETs
Differentiation

- Highest UIS rating
- High SCWT rating
- Low $R_{DS(on)}$
- Low ESR $R_g<1.5\Omega$
- Low $R_{DS(on)}$ variation over temperature
- Well-positioned in market
- Hi-Rel legacy (extreme environment, high performance aviation)
- Business
- Only major US-based SiC vendor (Defense/Space)
- Cost competitive

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SiC MOSFET: Design for Ruggedness

- High yield process, high reliability
- Excellent gate integrity, verified through TDDB* and HTGB**, high gate yield
- High UIS*** capability: ~ 10 -15 J/cm², ~1.5x - 2x higher than competition
- High short circuit rating ~2 µS - 4 µS, 1.5x - 5x higher than competition

* TDDB = Time Dependant Dielectric Breakdown
** HTGB = High Temperature Gate Bias
*** UIS = Unclamped Inductive Switching
RUlS-TDDB Gate Oxide Stress Tests Vs. Competition

- Two major metrics for comparison
  - Average time to breakdown
  - Dispersion of the lifetime distribution

- Microsemi’s robust next generation 1200 V, 40 mΩ SiC MOSFET
  - Excellent gate oxide shielding and channel integrity
  - No gate oxide lifetime degradation even after 100 K Repetitive-UIS

- Competitor devices showed degradations in either metrics compared to Microsemi SiC MOSFET

The TDDB test condition is constant current 50 uA @ room temperature

* RUIS = Repetitive Unclamped Inductive Switching
** TDDB = Time Dependant Dielectric Breakdown
Key Electrical Performance Needs

- Low Rdson (via large area dies) decreases component count and improves reliability
- Low Rdson variation over temperature – lowers requirements for cooling and reduces die count (~50-60% for SiC FETs vs. ~250% for Si superjunction)
“Average Star” Design Approach

- Datasheet parameters well centered (“Average”)
- Easy drop-in replacement to existing SiC designs
- Enables multiple vendor sourcing
- Differentiate (“Star”) via reliability and robustness
SiC MOSFETs have 10X lower FIT rate than comparable Si IGBTs @ rated voltage

Microsemi SiC MOSFETs perform well against competition re. neutron irradiation
### Next Generation SiC MOSFET Products

<table>
<thead>
<tr>
<th>Voltage</th>
<th>$R_{DS(on)}$(typical)</th>
<th>Part Number</th>
<th>Package</th>
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<tr>
<td>700 V</td>
<td>90 mΩ</td>
<td>MSC090SMA070B</td>
<td>TO-247</td>
</tr>
<tr>
<td></td>
<td>60 mΩ</td>
<td>MSC060SMA070B</td>
<td>TO-247</td>
</tr>
<tr>
<td></td>
<td>35 mΩ</td>
<td>MSC035SMA070B</td>
<td>TO-247</td>
</tr>
<tr>
<td></td>
<td>15 mΩ</td>
<td>MSC015SMA070B</td>
<td>TO-247</td>
</tr>
<tr>
<td>1200 V</td>
<td>280 mΩ</td>
<td>MSC280SMA120B</td>
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<td>140 mΩ</td>
<td>MSC140SMA120B</td>
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<td>80 mΩ</td>
<td>MSC080SMA120B</td>
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</tr>
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<td></td>
<td>40 mΩ</td>
<td>MSC040SMA120B</td>
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</tr>
<tr>
<td></td>
<td>25 mΩ</td>
<td>MSC025SMA120B</td>
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<td>1700 V</td>
<td>750 mΩ</td>
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<td></td>
<td>45 mΩ</td>
<td>MSC045SMA170B</td>
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</table>

- **Sampling**
  - MSC040SMA120B
- **AEC-Q101 planned for 1200 V and 700 V SiC MOSFETs**
Next-Generation SiC Diode Nomenclature

MSC 040 SMA 120 B

MSC = Microsemi Corporation

RDS_{ON}
015 = 15 mΩ
025 = 25 mΩ
035 = 35 mΩ
040 = 40 mΩ

S: Silicon Carbide (SiC)
M = MOSFET
A = Revision or generation

Package code
B = TO-247
K = TO-220
S = D^3PAK
J = SOT-227

Voltage
070 = 700 V
120 = 1200 V
170 = 1700 V
SiC Discrete diode
SiC Diodes: Design for Ruggedness

- Improved avalanche ruggedness for Unclamped Inductive Switching (UIS) rating.
- The design needs to be optimal such that the device breakdown under UIS needs to be:
  - constrained to happen in the active area instead of the terminations
  - uniform without the presence of prominent hotspots, indicating weak areas

Backside emission imaging of SiC SBD at the onset of avalanche
SiC Diodes: Design for Ruggedness

- Passed 1000hrs HTRB (960V, 175C), 10,000 power cycles (up to Tj=100C)
- High UIS capability
- R-UIS better indicator than single-shot UIS
- High R-UIS capability at >10K hits at rated current with no degradation or failures
“Average Star” Design Approach

- Datasheet parameters well centered ("Average")
- Easy drop-in replacement to existing SiC designs
- Enables multiple vendor sourcing
- Differentiate ("Star") via reliability and robustness

Datasheet comparisons normalized to Microsemi MSC10SDA120B 10 A/1200 V TO-247 SiC Diode

- Datasheet parameters well centered ("Average")
- Easy drop-in replacement to existing SiC designs
- Enables multiple vendor sourcing
- Differentiate ("Star") via reliability and robustness
## Next Generation SiC Schottky Barrier Diode Products

<table>
<thead>
<tr>
<th>Voltage</th>
<th>$I_{\text{avg}}$</th>
<th>$V_F$</th>
<th>Part Number</th>
<th>Package</th>
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<tbody>
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<td>700</td>
<td>10</td>
<td>1.5</td>
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<td></td>
<td></td>
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<td>MSC010SDA070B</td>
<td>TO-247</td>
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<tr>
<td></td>
<td>30</td>
<td>1.5</td>
<td>MSC030SDA070K</td>
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<td></td>
<td></td>
<td></td>
<td>MSC030SDA070B</td>
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<td>50</td>
<td>1.5</td>
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<tr>
<td>1200</td>
<td>10</td>
<td>1.5</td>
<td>MSC010SDA120B</td>
<td>TO-247</td>
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<td>MSC010SDA120K</td>
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<td></td>
<td>15</td>
<td>1.5</td>
<td>MSC015SDA120B</td>
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<td>30</td>
<td>1.5</td>
<td>MSC030SDA120B</td>
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<td></td>
<td></td>
<td></td>
<td>MSC050SDA120S</td>
<td>D³PAK</td>
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<td>1700</td>
<td>10</td>
<td>1.5</td>
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<td>50</td>
<td>1.5</td>
<td>MSC050SDA170B</td>
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</tbody>
</table>

### Sampling
- MSC010SDA120B
- MSC030SDA120B
- MSC050SDA120B

### AEC-Q101 qualification on going for 1200 V and 700 V SiC SBDs
Next-Generation SiC Diode Nomenclature

MSC 010 SDA 120 B

MSC = Microsemi Corporation

Current
010 = 10 A
015 = 15 A
030 = 30 A
050 = 50 A

S: Silicon Carbide (SiC)
D = Diode
A = Revision or generation

Package code
B = TO-247
K = TO-220
S = D³PAK
J = SOT-227

Voltage
070 = 700 V
120 = 1200 V
170 = 1700 V
SiC Power Modules
SiC power module allows higher power density

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Microsemi APTGLQ300A120G</th>
<th>Microsemi APTMC120AM20CT1AG</th>
<th>Comparison SiC vs Si</th>
</tr>
</thead>
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<tr>
<td>Semiconductor type</td>
<td>Trench4 IGBT</td>
<td>SiC MOSFET</td>
<td></td>
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<tr>
<td>Ratings @ Tc=25°C</td>
<td>500 A/1200 V</td>
<td>143 A/1200 V</td>
<td>~3.5 x lower</td>
</tr>
<tr>
<td>Package type</td>
<td>SP6 – 108x62 mm</td>
<td>SP1 – 52x41 mm</td>
<td>~3.0 x smaller</td>
</tr>
<tr>
<td>Current @ 30 kHz</td>
<td>130 A</td>
<td>130 A</td>
<td>-</td>
</tr>
<tr>
<td>Tc=75°C, D=50%, V=600 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current @ 50 kHz</td>
<td>60 A</td>
<td>115 A</td>
<td>~2.0 x higher</td>
</tr>
<tr>
<td>Tc=75°C, D=50%, V=600 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Eon+Eoff @ 100 A</td>
<td>16.0 mJ</td>
<td>3.4 mJ</td>
<td>~5.0 x lower</td>
</tr>
<tr>
<td>Tj=150°C, V=600 V</td>
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</tr>
</tbody>
</table>

MORE POWER @ HIGHER SWITCHING FREQUENCY in SMALLER VOLUME
Packaging and power density

- Low parasitic inductance package is essential to get all benefit for fast switching speed semiconductors as SiC.
- At 15 kA/µs typical switching speed the overvoltage is too high or switching speed must be reduced if parasitic inductance is too high.

<table>
<thead>
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<th>Package</th>
<th>Height</th>
<th>Stray Inductance</th>
<th>Overvoltage</th>
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<tbody>
<tr>
<td>D3</td>
<td>30 mm</td>
<td>30 nH</td>
<td>450 V</td>
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<tr>
<td>SP6</td>
<td>17 mm</td>
<td>15 nH</td>
<td>225 V</td>
</tr>
<tr>
<td>SP6P</td>
<td>12 mm</td>
<td>5 nH</td>
<td>75 V</td>
</tr>
</tbody>
</table>

Lowest inductance will allow fastest driving, best efficiency and safe operation.
Very low inductance package: Objectives

- Develop a standard package targeting <5 nH stray inductance to be used in high switching frequency applications with SiC semiconductors.

- Offer a standard footprint package recognized on the market.

- Benefit from one layout to use different die vendors to compare easily different performances and make the right choice for the application.
Very low inductance package: Realization

- Optimized layout for multi SiC MOSFET and Diode chips assembly in phase leg topology.
- Symmetrical design to accept up to 12 SiC MOSFET chips in parallel per switch to offer a total $R_{\text{DS\text{ON}}} \text{ down to } 2 \, \text{m}\Omega \text{ per switch.}$
- All die in parallel with its own gate series resistor for homogenous current balancing.
- High current capability up to 600A at very fast switching frequency.
- Optional mix of assembly materials to better address various markets and applications:
  - AlN or Si3N4 substrates
  - Copper or AlSiC baseplates
  - Pin fins base plate option for direct liquid cooling
Very low inductance package: Description

SP6LI package
- Very low stray inductance
- High frequency performance
- 1200V & 1700V SiC MOSFET & anti-parallel Diode
- Rdson down to 2 mΩ
- Screw terminals for signal & power
- Phase leg configuration
- AlN or Si3N4 substrate
- Copper or AlSiC baseplate
- Temperature sensor (NTC)
- Standard package footprint 62 x 108 mm
- 17 mm height
The very low stray inductance is achieved thanks to:

- Connections to the substrate as close as possible to the chips
- Bus bars for DC connections
- Strip line design for DC link
- Symmetrical Layout
The stray inductance of the DC link is simulated with the software Comsol. The signal is applied between the two screw locations for Vbus and the return O/Vbus.

The parasitic inductance varies from 3.58 nH at 100 KHz to 3.38 nH at 1 MHz and confirms good values well below the 5 nH target.

Homogeneous temperature distribution for both the SiC Mosfet and SiC diode devices and confirms a $R_{thjc \ max} = 0.057 \ K/W$ for the SiC Mosfet and $0.112 \ K/W$ for the SiC diode.

High frequency current homogeneous distribution on the substrate.
Very low inductance package: Test results

DC bus connections must be routed to the module with very low parasitic inductance.

- A decoupling PCB is mounted on the module with the DC connections distributed in strip line.
- Ceramic capacitors are mounted as close as possible from the power connections.
- A window is open in the PCB to insert a rogowski current probe to monitor the switch current.

- $V_{bus}$ is measured on the power connectors.
- $V_{chip}$ is measured on the substrate as close as possible of the power die.
- $dV = V_{chip} - V_{bus} = 75$ V
- $di/dt = 25.7$ A/ns

Module stray inductance
$L_s = 2.9$ nH
Very low inductance package: Test Results

MSCMC120AM02CT6LINMG – 1200 V/2 mΩ full SiC Phase Leg with AlSiC base plate and Si3N4 substrates

Operating Frequency vs Drain Current

**Vbus = 600 V**

Id = 600 A

Tj = 150°C

Eon = 8.9 mJ

Eoff = 5.2 mJ

Eon = 8.9 mJ

Eoff = 5.2 mJ

Hard Switching capabilities

540 A @ Fsw = 50 kHz

400 A @ Fsw = 100 kHz

230 A @ Fsw = 200 kHz
Very low inductance package: Test Results

MSCMC120AM02CT6LINMG – 1200 V/2 mΩ full SiC Phase Leg with AlSiC base plate and Si3N4 substrates

- Very low $R_{dson}$:
  - ~ 4.0 mΩ at $T_J = 150^\circ$C in the forward direction
  - ~ 2.5 mΩ at $T_J = 150^\circ$C in the third quadrant assuming $V_{GS} = 20V$ and $I_D = 600A$
3 phase configuration – flexible assemblies

3 x SP6LI power modules can be connected horizontally or vertically with DC bus bars to achieve a 3 phase configuration

- The best recommendation is to place the modules side by side in the length.
- Distribute the +DC and – DC link via bus bars in strip line that include the capacitor bank.
- In this configuration the DC link distribution is very symmetrical and with very low stray inductance.

- Other alternative is to place the modules side by side in the width
- Distribute the +DC and – DC link via bus bars in strip line
Paralleling SP6 Low Inductance modules

- If a PCB is used to interconnect the modules, ceramic decoupling capacitors should be placed as close as possible from the power terminals for improved stray inductance.
- Layout should be achieved in strip line to achieve minimum parasitic inductance.
- Gate drive signals should also be routed in strip line for minimum parasitic inductance in the control path.
New standard parts

<table>
<thead>
<tr>
<th>PN</th>
<th>Voltage</th>
<th>Current Tc=80°C</th>
<th>Rdson Typ Tj=25°C</th>
<th>Rdson max. Tj=25°C</th>
<th>SiC parallel diode ratings</th>
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<tbody>
<tr>
<td>MSCMC120AM07CT6LIAG</td>
<td>1200 V</td>
<td>210 A</td>
<td>6.7 mΩ</td>
<td>9.2 mΩ</td>
<td>100 A</td>
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<td>MSCMC120AM04CT6LIAG</td>
<td>1200 V</td>
<td>307 A</td>
<td>4.2 mΩ</td>
<td>5.6 mΩ</td>
<td>200 A</td>
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<td>MSCMC120AM03CT6LIAG</td>
<td>1200 V</td>
<td>475 A</td>
<td>2.5 mΩ</td>
<td>3.4 mΩ</td>
<td>250 A</td>
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<tr>
<td>MSCMC120AM02CT6LIAG</td>
<td>1200 V</td>
<td>586 A</td>
<td>2.1 mΩ</td>
<td>2.8 mΩ</td>
<td>300 A</td>
</tr>
<tr>
<td>MSCMC170AM08CT6LIAG</td>
<td>1700 V</td>
<td>207 A</td>
<td>7.5 mΩ</td>
<td>11.7 mΩ</td>
<td>200 A</td>
</tr>
</tbody>
</table>
MSC MC 120 A M02 C T 6LI A _ G

**MSC** = Trade mark

**Semiconductor type:**
- **SM** = MSC SiC MOSFET
- **MC** = Wolfspeed

**Breakdown Voltage:**
- **70** = 700 V
- **120** = 1200 V
- **170** = 1700 V

**Rdson:**
- **M02** = 02 mOhms
- **M03** = 03 mOhms
- **M08** = 08 mOhms

**Electrical topology:**
- **A** = Phase Leg

**Baseplate Material:**
- **M** = AlSiC
  - **Left blank** = Copper

**Substrate Material:**
- **A** = AlN
- **N** = Si3N4

**Package:**
- **6LI** = SP6 Low Inductance

**Temperature Sensor:**
- **T** = Thermistor (NTC)
  - **Left blank** = no NTC

**Anti-parallel Diode:**
- **C** = added SiC Diode
  - **Left blank** = no diode

**G** = RoHS compliant
# SiC MOSFET module

<table>
<thead>
<tr>
<th>Technology</th>
<th>Topology</th>
<th>BVDS</th>
<th>Current Tc=80°C</th>
<th>Rdson max. per switch Tj=25°C</th>
<th>Package</th>
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<tr>
<td>APTMC120TAM34CT3AG</td>
<td>3-Phase leg</td>
<td>1200 V</td>
<td>55 A</td>
<td>34 mΩ</td>
<td>SP3F</td>
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<td>58 A</td>
<td>33 mΩ</td>
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<td>110 A</td>
<td>17 mΩ</td>
<td>SP6P</td>
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<td>80 A</td>
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# SiC MOSFET module

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<tr>
<th>PART NUMBER</th>
<th>TOPOLOGY</th>
<th>BVDS</th>
<th>Id (A) @ Tc=80°C (A)</th>
<th>RdsON @ Tj=25°C</th>
<th>NTC</th>
<th>PACKAGE</th>
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<td>160 A</td>
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# SiC Diode module

## Specifications

### 600 V

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<tr>
<th>V&lt;sub&gt;RRM&lt;/sub&gt;</th>
<th>Module Type</th>
<th>I&lt;sub&gt;F&lt;/sub&gt;</th>
<th>V&lt;sub&gt;F&lt;/sub&gt;</th>
<th>Package</th>
<th>Anti-Parallel Configuration</th>
<th>Parallel Configuration</th>
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<td>SOT-227</td>
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### 1200 V

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<th>V&lt;sub&gt;F&lt;/sub&gt;</th>
<th>Package</th>
<th>Anti-Parallel Configuration</th>
<th>Parallel Configuration</th>
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<tbody>
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<td>1.6 V</td>
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<td>SOT-227</td>
<td>APT2X60DC120J</td>
<td>APT2X61DC120J</td>
</tr>
</tbody>
</table>

## Additional Information

- **V<sub>RRM</sub>**: Rated Reverse Voltage
- **I<sub>F</sub>**: Forward Current
- **V<sub>F</sub>**: Forward Voltage
- **Package**: SOT-227

### Full Bridge

<table>
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<tr>
<th>V&lt;sub&gt;RRM&lt;/sub&gt;</th>
<th>Module Type</th>
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<th>V&lt;sub&gt;F&lt;/sub&gt;</th>
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<th>Part Number</th>
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</tbody>
</table>

## Links


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SiC gate driver boards
SiC Module Reference Design Driver
SP3 Power Module Reference Design (MSCSICSP3/REF2)

- Half Bridge Driver
- Up to 400 kHz switching frequency
- 12 V $V_{IN}$ supply
- Capable of 16 W of gate drive power / side
- 30 A Peak Source output current
- Min.100 KV/$\mu$S CMTI
- -5 V/+20 V output gate drive
- Low propagation delay variability
- Fault signaling
- Under voltage lockout protection
- Programmable dead time protection
- Desaturation protection
- Screw output terminals

SiC Module Reference Design Driver
SP6LI Power Module Reference Design (MSCSICSP6/REF3)

- Featuring brand **new SP6LI** (Low Inductance)
  - Stray inductance < 3 nH to fully benefit from SiC
  - Designed to be easy to parallel
  - Up to 1200 V and 586 A
- Half Bridge Driver
- Up to 400 kHz switching frequency
- 12 V VIN supply
- Capable of 16 W of gate drive power / side
- 30 A Peak Source output current
- Min.100 KV/µS CMTI
- -5 V/+20 V output gate drive
- Low propagation delay variability
- Fault signaling
- Under voltage lockout protection
- Programmable dead time protection
- Desaturation protection

SiC Module Reference Design Driver
SP1 Power Module Reference Design

- Half Bridge Topology with SiC
  - APTMC120AM20CT1AG
  - APTMC120AM55CT1AG
- 1200 V, 50 A, 200 kHz
- >100 kV/us CMTI
- 12 V VIN supply
- Independent High Side and Low Side PWM inputs (Single control with 70ns deadtime for testing)
- 1xLT3999 + 1xADuM4135 for both High Side and Low Side
- Full tested ‘Desat protection’
- Low inductive and high current terminals for V+, V- and AC phase connection

NEW!
Aerospace Integrated Power Solutions
Power Core Module (PCM)  
Actuation Motor Drive Solution using SiC MOSFETs and/or IGBTs

- 5 kVA (540 VDC) 3-phase power inverter
- Designed per Airbus standard PCM specification for flight critical actuation drive
  - Line Replaceable Unit (LRU)
- Full reliability analysis complete
  - Life testing in progress
- Passed all DO-160 Environmental and EMC
- Proven building blocks allow for fast turnaround for customized high reliability solutions
- On-board telemetry monitoring and communication bus

Evaluation Kit Available!!

www.microsemi.com/pcm

www.microsemi.com/ips
Hybrid Power Drive (HPD510 or HPD520)
3 Phase Inverter with Integrated Gate Drive using SiC MOSFETs or IGBTs

- 5 kVA – 20 kVA scalable solutions
- HPD = Hybrid Power Substrate + Integrated Drive
  - Telemetry and control added at the PCM level
- Solutions proven with SiC MOSFETs but can be tailored to IGBT
- HPD510 qualified through Airbus PCM qualification
  - Line Replaceable Unit (LRU)
- HPD520 designed in collaboration with SAFRAN in support of Actuation2015 consortium
  - Fully integrated PCB mounted solution
- Partial Discharge Effects Evaluated

Hybrid Power Drive (HPD510)
www.microsemi.com/hpd

Hybrid Power Drive (HPD520)
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